Karunya University
(Karunya Institute of Technology and Sciences)
(Declared as Deemed to be University under Sec.3 of the UGC Act, 1965)

End Semester Examinations - 2015-16 Even Semester - May 2016

14EC3026 Testing And Testability

Set B

Time : 3 hrs
Total Marks: 100

1. 1. a. Define Fault detection and Fault diagnosis. (4)

b. Use D-algorithm for generating test pattern for line 5 s-a-0 for the Figure (1) shown below. (16)

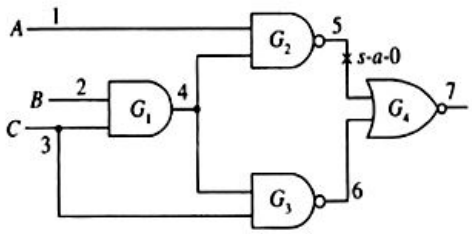

Figure (1)

OR

2. 2. a.Differentiate between testing and verification. (4)

b. Use Boolean difference method to generate test patterns for detecting the fault in the circuit given in Figure (2) with respect to variable h. (16)

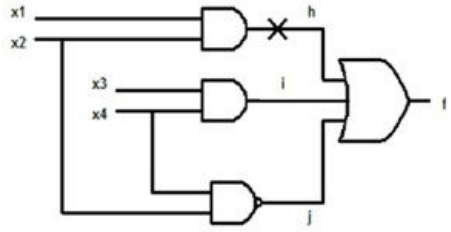

Figure (2)

3. 3. a. Justify that testing cost decides the yield of a chip. (4)

b. Consider all possible stuck at faults in the circuit of Figure (3), apply fault equivalence and reduce the number of faults and indicate the collapse ratio. (16)

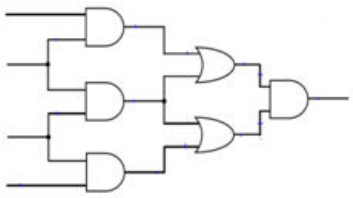

Figure (3)

OR

4. 4. a. With example define defect, fault and error. (4)

b. Find the minimal test vectors for the circuit shown in Figure (4) using fault table method. (16)

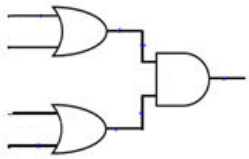

Figure (4)

5. 5. Derive the test sequence for the state table of the sequential circuit shown in Table 1 using checking experiment. (20)

Table 1

PS	X=0	X=1
A	A/1	E/0
B	A/0	C/0
C	B/0	D/1
D	C/1	C/0
E	C/0	D/0

OR

6. 6.a. Indicate the algorithmic steps of serial fault simulation. (4)

b. With example, illustrate parallel fault simulation technique. (16)

7. 7.a. Describe the various Ad Hoc design rules for improving testability. (6)

b. With necessary diagrams explain LSSD design rules. (14)

OR

8. 8.a. Define Observability. (2)

b. With necessary block diagrams describe in detail about Boundary Scan Technique. (18)

9. 9.a. With necessary diagrams describe in detail about circular BIST. (12)

b. Explain about STUMPS BIST architecture. (8)

Wishing you All the Best
